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(71) Applicant(s)
NEC Corporation

(Incorporated in Japan)

7-1 Shiba 5-chome, Minato-ku, Tokyo, Japan

(72) Inventor(s)
Sachiko Oguri

(74) Agent and/or Address for Service
Mathys & Squire
100 Grays Inn Road, LONDON, WC1X 8AL,
United Kingdom

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B3V V4A2B

(56) Documents Cited
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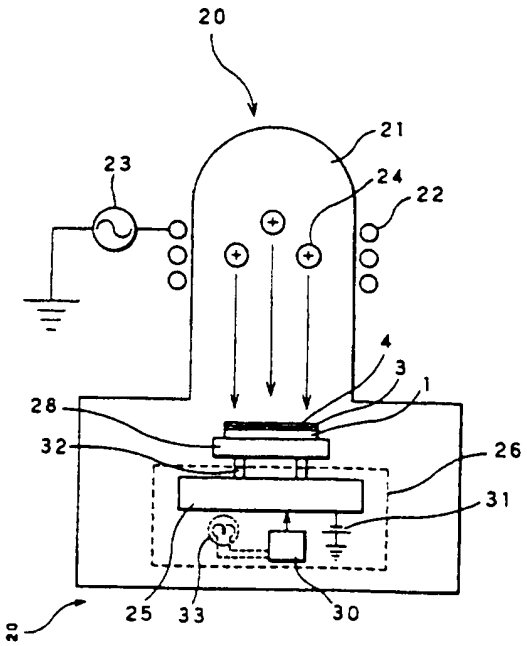
EP 0304068 A US 5268056 A US 5226056 A

(58) Field of Search
UK CL (Edition P) G2X XB5D , H1K KLX
INT CL^6 G03F , H01L

(54) Removing a resist film

(57) A hardened layer 4 formed over unhardened layer 3 of a resist film 2, layer 4 is formed as a result of ion implantation of a semiconductor substrate 1 is removed by bombarding the layer with positively charged ions, e.g. of oxygen, an oxygen/hydrogen mixture, argon or helium generated by an hf coil 22, the substrate being negatively biased by electrode 25 and the temperature being low enough to avoid popping. The temperature may be 120°C or below, the substrate being heated by heater such as a lamp 33. After removal of the hardened layer, layer 3 of the resist film can be removed by bombardment with the same ions, but with the substrate being unbiased and at an elevated temperature, e.g. 150-300°C. Temperature control may be effected by using pins 32 to vary the distance between the heater 33 and the substrate 1.

FIG. 7



GB 2 320 335

FIG. 1A

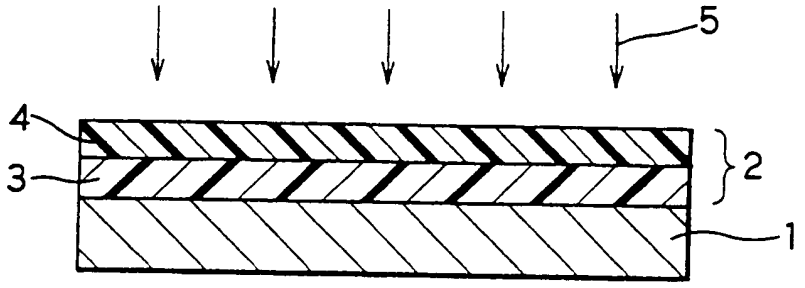


FIG. 1B

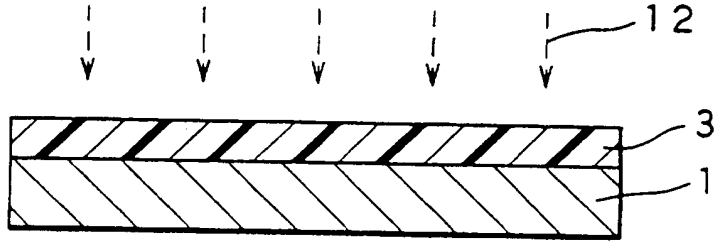


FIG. 1C

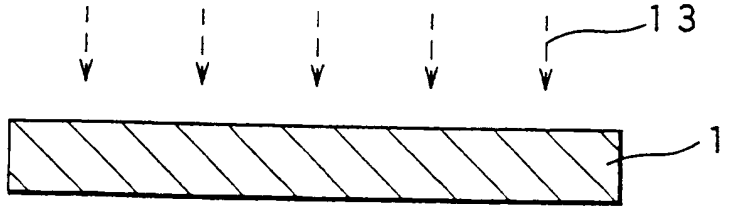


FIG. 2A

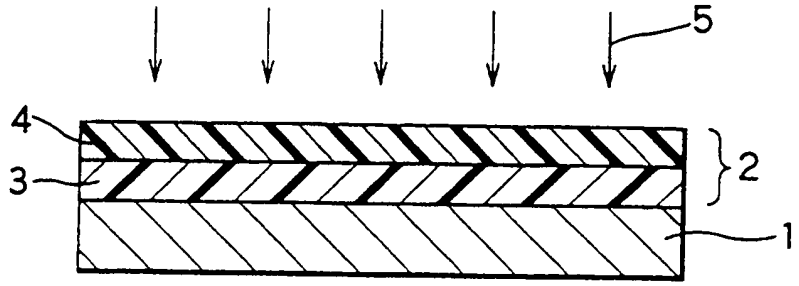


FIG. 2B

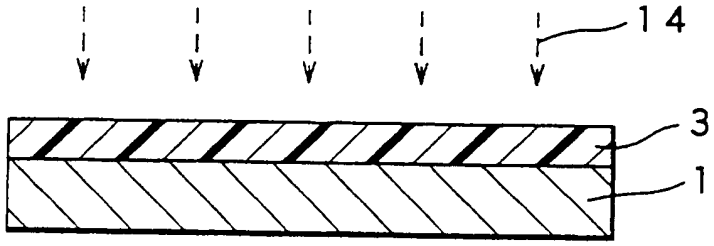


FIG. 2C

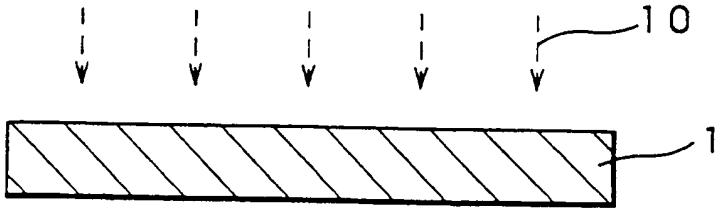


FIG. 3A

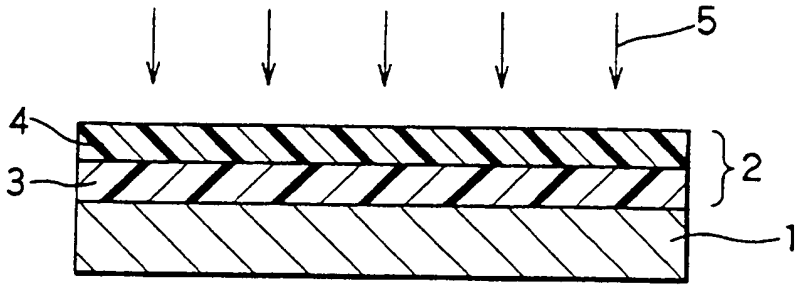


FIG. 3B

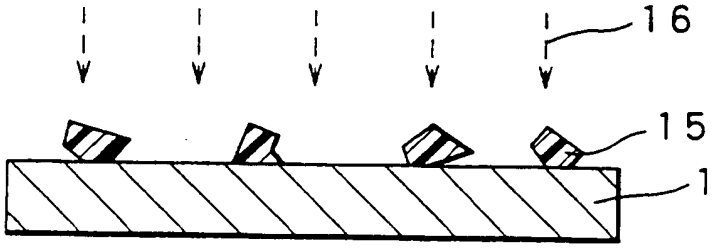


FIG. 3C

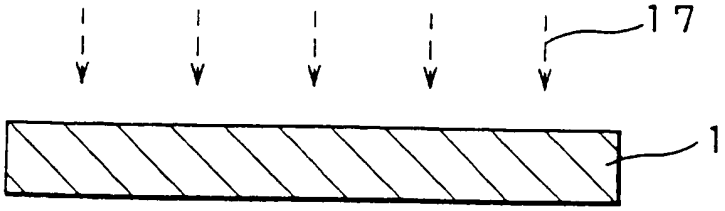


FIG. 4A

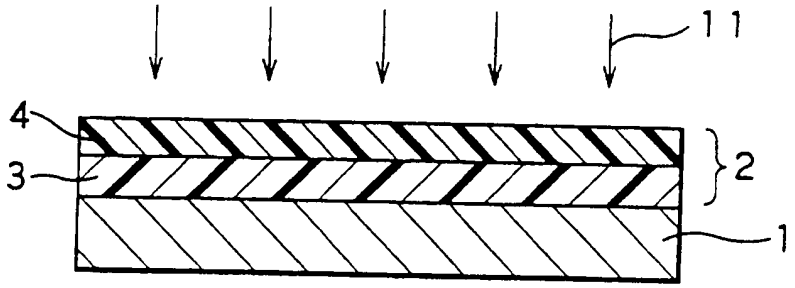


FIG. 4B

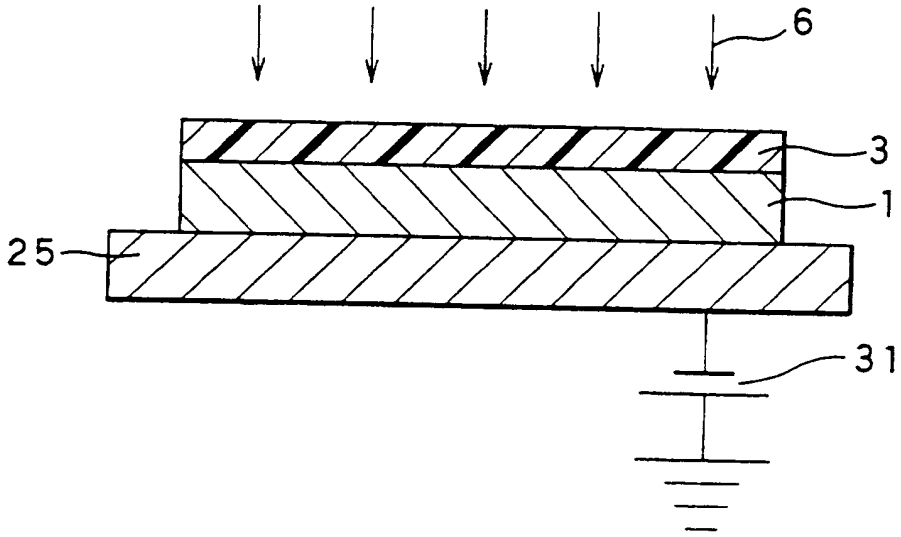


FIG. 4C

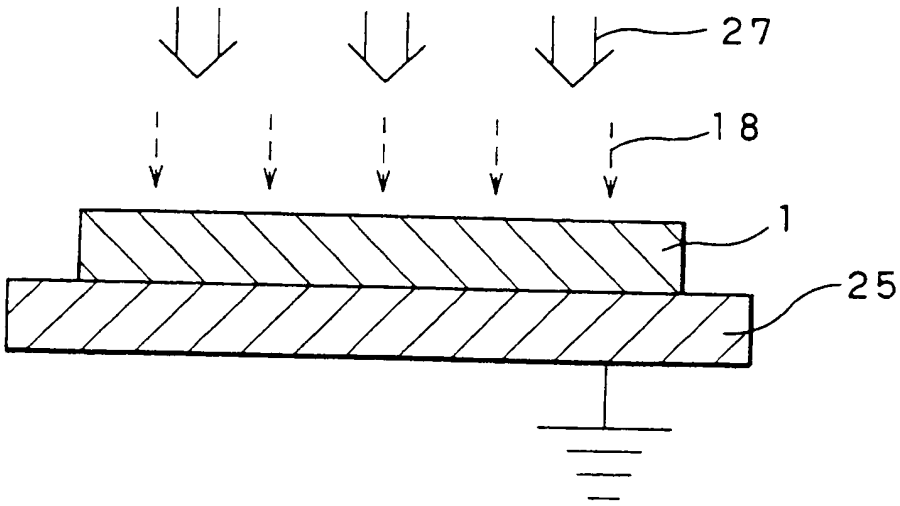


FIG. 5A

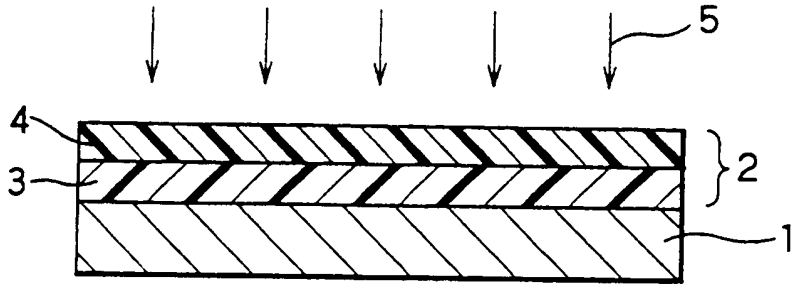


FIG. 5B

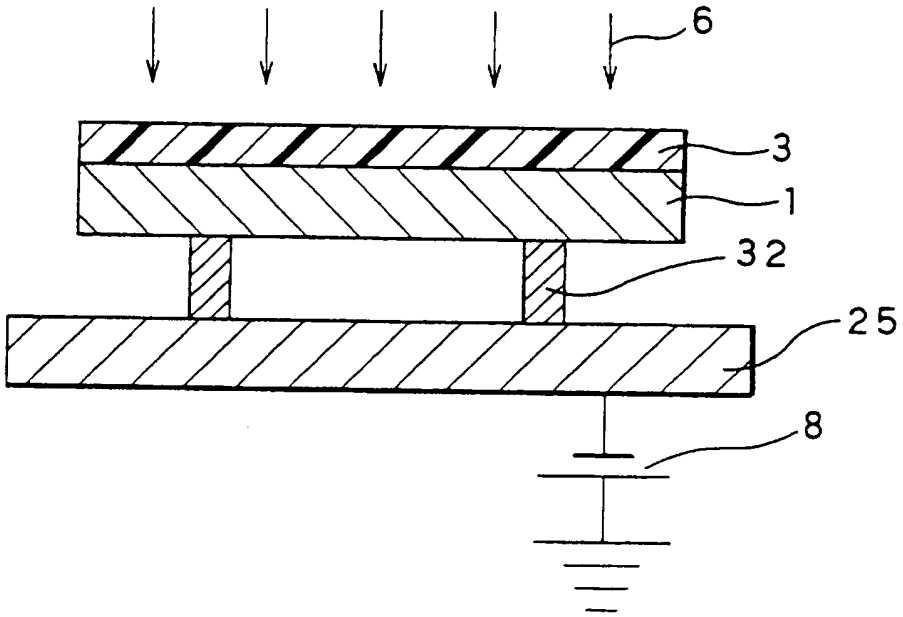


FIG. 5C

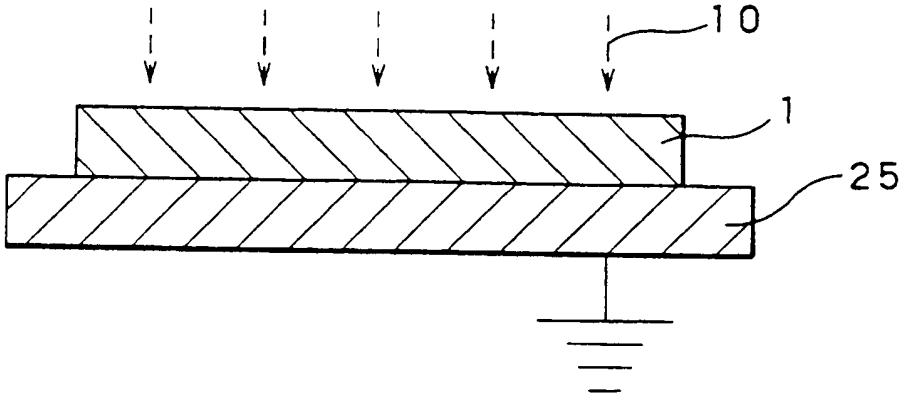


FIG. 6

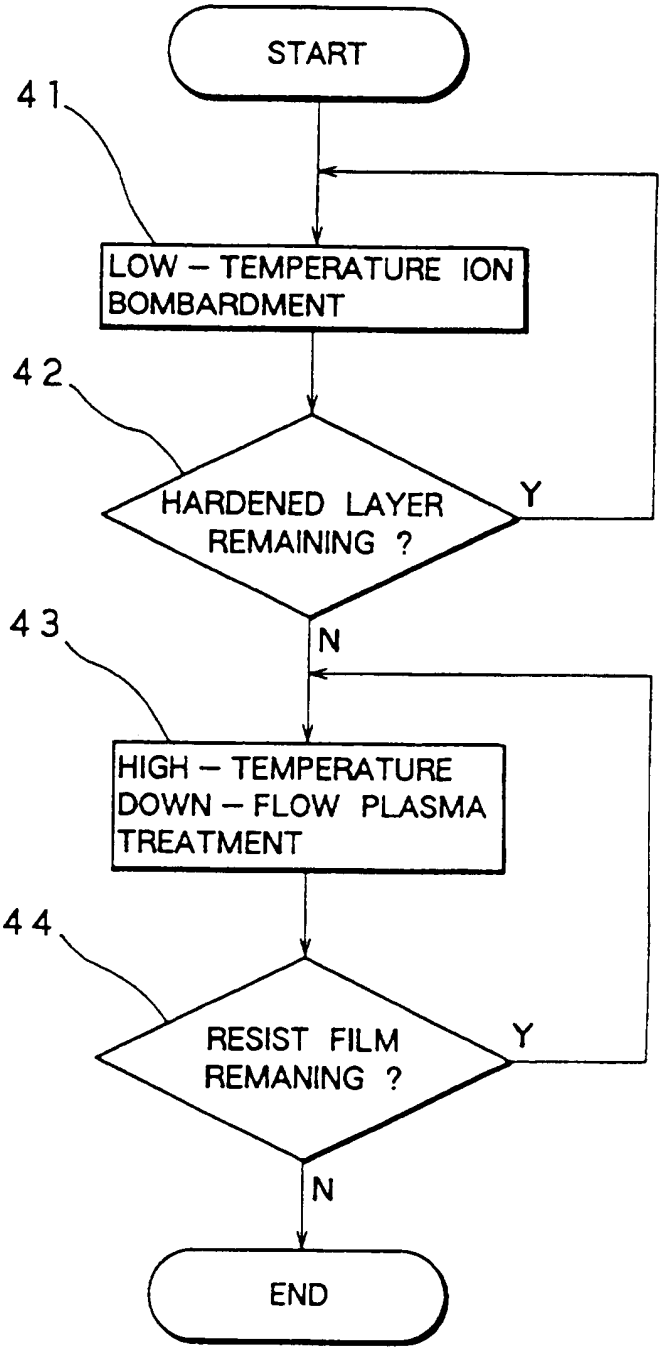

START
41
LOW – TEMPERATURE ION BOMBARDMENT
42
HARDENED LAYER REMAINING ?
Y
N
43
HIGH – TEMPERATURE DOWN – FLOW PLASMA TREATMENT
44
RESIST FILM REMANING ?
Y
N
END

FIG. 7

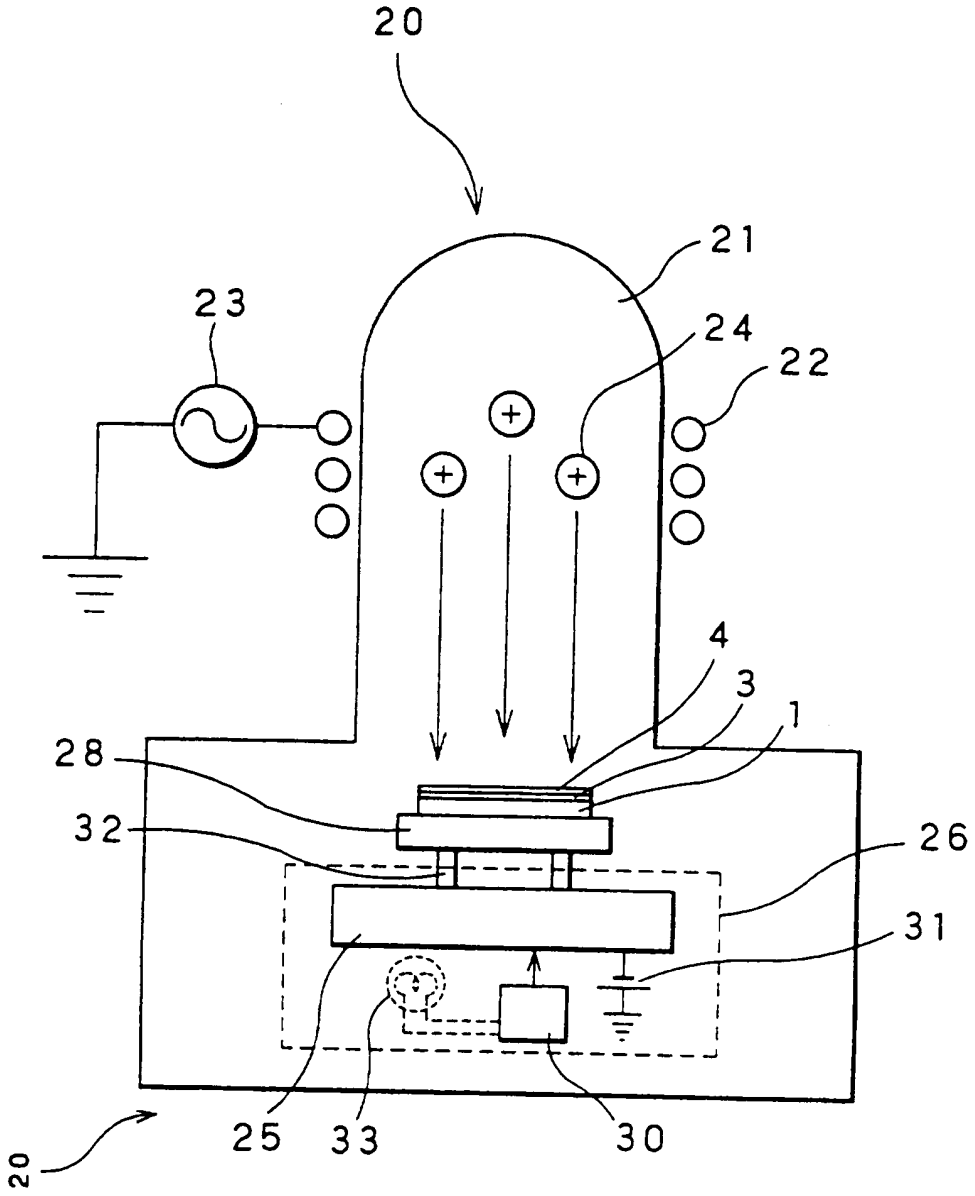
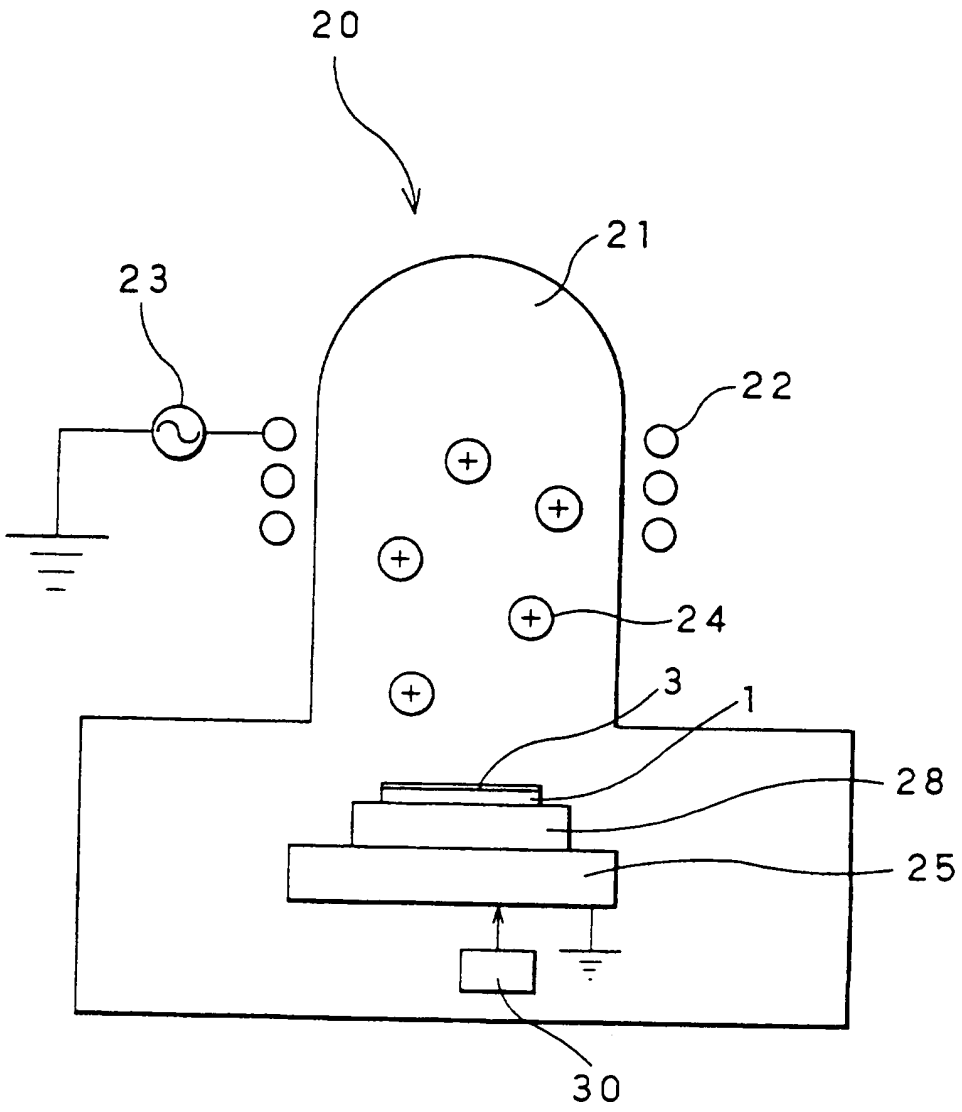


FIG. 8



2320335

TITLE OF THE INVENTION

METHOD AND APPARATUS FOR REMOVING RESIST FILM HAVING HARDENED LAYER

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method and apparatus for removing a resist film in a case where a surface layer of the resist film is hardened by ion implantation at a high dose, and, more particularly, to a method and apparatus for removing a resist film having a hardened layer, which can suppress the occurrence of popping.

Description of the Related Art

In the fabrication of a semiconductor device, a photoresist film is used as a mask at the time of dry etching or ion implantation. This photoresist film is frequently peeled or removed. The recent trend for the fabrication of semiconductor devices has moved to a dry process from a wet process, and ashing using oxygen plasma is mainly used even in removing of a resist film.

In removing or peeling a resist film by ashing, a resist film which is used in ordinary dry etching is peeled relatively easily. Since a resist film which is used as a mask in the step of injecting a high dose of ions has a hardened layer formed at its surface, the hardened layer cannot easily removed by an ordinary removing technique. This results in slower removing of the resist film.

Further, when heat is applied to the resist film having the hardened layer formed at its surface, popping may occur. The "popping" or violent rupture of the hardened layer is a phenomenon such that the hardened layer at the surface of the resist film bursts, widely scattering the residue of the resist film on the wafer. Popping is considered to be due to vaporisation and outgassing. of the remaining solvent contained in regions of the resist film other than the hardened layer. When popping occurs, the scattered residual of the resist film (popping residual) sticks on a semiconductor device or on the inner wall of a chamber where the semiconductor device is placed, thus degrading the quality and performance of the semiconductor device. When popping occurs, it is necessary to process the residual of the resist film. This complicates the fabrication of semiconductor devices. That is, as the popping residual significantly lowers the yield of semiconductor devices, it is necessary to suppress the occurrence of popping or to completely remove the popping residual in the ashing process.

As apparent from the above, the removing of the hardened layer at the surface of the resist film, the hardened layer having been formed by ion implantation, lowers the removal speed of the resist film. If the temperature of the resist film is raised to increase the removal speed as done in the ordinary ashing process, popping occurs.

Unexamined Japanese Patent Publication No. Hei 5-275326 discloses method for ashing resist, different from

the ordinary ashing, which is designed to prevent the occurrence of popping. This ashing method is hereinafter called first prior art. FIGS. 1A through 1C are cross-sectional views showing a step by step method for ashing resist according to the first prior art. As shown in FIG. 1A, an insulation oxide film (not shown) is formed on a semiconductor substrate 1, with a resist film 2 formed on this insulation oxide film. First, when a high dose of predetermined ions 5 is injected in the semiconductor substrate 1, a hardened layer 4 is formed at the surface of the resist film 2. That is, the resist film 2 consisting of the hardened layer 4 and an unhardened layer 3 is formed.

Next, ashing is carried out by using plasma 12 of a mixed gas consisting of an oxygen gas and fluorine-based gas, as shown in FIG. 1B. At this time, the activation energy of the hardened layer 4 is reduced by fluorine radicals consisting of a fluorine-based gas. This increases the ashing speed to remove the hardened layer 4 of the resist film 2.

Then, ashing is carried out using an oxygen plasma 13 to remove the unhardened layer 3 of the resist film 2, as shown in FIG. 1C. Since an oxygen gas alone is used in this step, etching of the base layer (insulation oxide film) is suppressed.

Unexamined Japanese Patent Publication No. Sho 64-48418 discloses an ashing method capable of removing a resist film by using a downstream ashing process. This ashing method will hereinafter be called second prior art.

FIGS. 2A through 2C are cross-sectional views illustrating a step by step ashing method according to the second prior art. To avoid the redundant and detailed description, like or same reference numerals are given to those components of the second prior art shown in FIGS. 2A-2C which are the same as the corresponding components of the first prior art shown in FIGS. 1A-1C. As shown in FIG. 2A, as a high dose of predetermined ions 5 is injected, a hardened layer 4 and an unhardened layer 3 are formed on a semiconductor substrate 1.

Next, ashing is performed on the hardened layer 4 of the resist film 2 by using an oxygen-free and hydrogen-containing gas 14. As a result, the chemical bonding of the dopant with the elements constituting the resist film in the hardened layer 4 is broken by an active seed in the H_2 plasma consisting of the hydrogen-containing gas 14. This active seed is coupled to the dopant to produce a volatile hydride, thereby removing the hardened layer 4.

Then, the unhardened layer 3 of the resist film 2 is removed by downstream ashing or wet separation by using oxygen gas 10 containing carbon tetrafluoride as shown in FIG. 2C.

According to the first and second prior arts, as apparent from the above, ashing is carried out in two stages to be able to efficiently remove the hardened layer 4 without etching the base layer (insulation oxide film).

Unexamined Japanese Patent Publication No. Hei 6-104223 discloses removal method of resist. This removal

method will hereinafter be called third prior art. FIGS. 3A through 3C are cross-sectional views illustrating a step-by-step removal method of resist according to the third prior art. To avoid the redundant and detailed description, like or same reference numerals are given to those components of the third prior art shown in FIGS. 3A-3C which are the same as the corresponding components of the first prior art shown in FIGS. 1A-1C.

As shown in FIG. 3A, as a high dose of ions 5, such as phosphorus, is injected in a resist film 2, a hardened layer 4 and an unhardened layer 3 are formed on a semiconductor substrate 1.

Next, ashing of the resist film 2 is carried out using a mixed gas 16 of an oxygen gas and nitrogen gas, as shown in FIG. 3B. As popping occurs at this time, a popping residual 15 sticks on the semiconductor substrate 1.

Then, a plasma treatment is executed by using a mixed gas 17 of an O_2 gas and SF_6 gas as shown in FIG. 3C. The amount of fluorine radicals produced in the plasma can be controlled by using the SF_6 gas, not a fluorocarbon compound. This plasma treatment can therefore allow an oxide of the dopant contained in the popping residual 15 to be decomposed by the fluorine radicals, thus removing that oxide.

According to the third prior art, the popping residual produced by the ordinary ashing process is decomposed and removed. Therefore, the popping residual 15 is removed completely, thereby preventing the quality and

performance of the semiconductor device from degrading.

The first to third prior arts however have the following shortcomings. While the supply of the fluorine-based gas is inhibited after removal of the hardened layer 4 or the fluorine radicals are prevented from becoming excessively large by using the SF_6 gas according to the first and third prior arts which use the fluorine-based gas, neither method can completely prevent the fluorine-based gas from damaging the base layer. In other words, those two prior arts have the problem that while the fluorine radicals can effectively remove the hardened layer 4, they also etch out the insulation oxide film formed on the surface of the semiconductor substrate 1.

Since the second prior art uses the combination of reactive dry etching (RIE) and downstream ashing, it requires both an RIE system and an ashing system. This increases the cost and reduces the throughput.

SUMMARY OF THE INVENTION

Accordingly, it is an object of at least the preferred embodiments of the present invention to provide a method and apparatus for removing a resist film having a hardened layer, which can prevent the occurrence of popping at a low cost without damaging the base layer even when a hardened layer is formed at the surface of the resist film by high-dose ion implantation in the resist film.

In one aspect the invention provides a method of removing a hardened layer of a resist film on a surface of a semiconductor substrate, comprising providing positively charged ions, maintaining the surface negatively biassed relative to said ions, and at a temperature low enough to avoid popping (as hereinbefore defined), and bombarding the hardened layer with said ions to remove it.

In another aspect, a method of removing a resist film having a hardened layer according to this invention comprises a step of removing a hardened layer at a surface of a resist film

formed on the semiconductor substrate. Said hardened layer is removed by low-temperature ion bombardment in which a surface of the semiconductor substrate is negatively charged kept at 120 °C or below and positively charged ions are showered onto the surface of the semiconductor substrate. This hardened layer is formed by ion implantation in the resist film. The low-temperature ion bombardment may include a step of keeping a temperature of the semiconductor substrate at 120 °C or below, a step of generating ions to be bombarded on the resist film, and a step of applying a bias to the ions. The application of a bias to the ions causes the ions to be showered on the surface of the resist film. Thereby, the hardened layer is removed. Further, the ions in use can be produced by one kind of gas selected from an oxygen gas, a mixed gas of an oxygen gas and nitrogen gas, an argon gas and a helium gas.

The method of removing a resist film having a hardened layer according to this invention can comprise, after the step of removing the hardened layer, a step of removing the remaining resist film, after removal of the hardened layer, by a down-flow plasma treatment in which no bias is applied to the ions. It is preferable that the temperature of the semiconductor substrate should be kept higher than that of the semiconductor substrate in the low-temperature ion bombardment.

An apparatus for removing a resist film having a hardened layer according to this invention comprises a closed chamber, an ion generator for generating ions in the

closed chamber, a bias applying device for applying a bias to positively charged ions with a surface of a semiconductor substrate negatively charged, and a temperature controller for controlling a temperature of the semiconductor substrate. The semiconductor substrate is placed in the closed chamber. The bias applying device can form such an electric field as to accelerate the ions toward the resist film on the semiconductor substrate. Further, the temperature controller may have a heat source for heating the semiconductor substrate. Furthermore, the temperature controller may have a distance adjuster for adjusting a distance between the semiconductor substrate and the heat source.

According to this invention, when the surface of the resist film on the semiconductor substrate is hardened by ion implantation, thus forming a hardened layer, this hardened layer is removed by low-temperature ion bombardment. When positively charged ions hit against the hardened layer then, the chemical bond in the hardened layer is efficiently broken up by the ions, generating volatile hydride. This can allow the hardened layer to be easily removed. When ions having a high activity like fluorine ions are used in the step of removing the hardened layer, an interlayer insulator film or the like formed on the surface of the semiconductor substrate may be damaged. If the temperature of the semiconductor substrate is raised to remove the hardened layer without using ions having a high activity, popping occurs. The popping degrades the

quality and performance of semiconductor devices and reduces the yield of the semiconductor devices. Since this invention employs low-temperature ion bombardment in which positively charged ions are showered on the negatively charged surface of the semiconductor substrate while keeping the semiconductor substrate at 120 °C or lower, it is possible to remove the hardened layer at a temperature lower than that of the semiconductor substrate in the conventional ashing process without using ions with a high activity. This method can therefore prevent the occurrence of popping and the surface of the semiconductor substrate from being damaged by the ions, thus improving the yield of semiconductor devices.

According to this invention, after removal of the hardened layer, the remaining resist film can be removed by the down-flow plasma treatment in which no bias is applied to the ions. Because the hardened layer is completely removed in this step, even if the semiconductor substrate is kept at a temperature higher than the substrate temperature in the low-temperature ion bombardment, the resist film can be removed without causing popping.

Since the low-temperature ion bombardment and down-flow plasma treatment can be carried out in the same chamber using the same ions according to this invention, the hardened layer and the remaining resist film can be removed successively, thereby contributing to the reduction of the production cost.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A through 1C are cross-sectional views showing a step by step method for ashing resist according to the first prior art;

FIGS. 2A through 2C are cross-sectional views illustrating a step by step ashing method according to the second prior art;

FIGS. 3A through 3C are cross-sectional views illustrating a step-by-step removal method of resist according to the third prior art;

FIGS. 4A through 4C are cross-sectional views showing a step-by-step method of removing a resist film having a hardened layer according to the first embodiment of this invention;

FIGS. 5A through 5C are cross-sectional views illustrating a step-by-step method of removing a resist film having a hardened layer according to the second embodiment of the invention;

FIG. 6 is a flowchart illustrating the removing method of the resist film embodying the invention;

FIG. 7 is an exemplary diagram of an apparatus for removing a resist film according to the first embodiment of the invention; and

FIG. 8 is an exemplary diagram showing an apparatus for removing a resist film according to the second embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of this invention will specifically be described below by way of example only with reference to the

accompanying drawings. FIGS. 4A through 4C are cross-sectional views showing a step-by-step method of removing a resist film having a hardened layer according to the first embodiment of this invention. As shown in FIG. 4A, an insulation oxide film (not shown) is formed on a semiconductor substrate 1, and a resist film 2 is formed on this insulation oxide film. First, when a high dose of arsenic ions (As^+) 11 is injected in the semiconductor substrate 1, a hardened layer 4 is formed at the surface of the resist film 2. That is, the resist film 2 consisting of the hardened layer 4 and an unhardened layer 3 is formed.

Next, the hardened layer 4 of the resist film 2 is removed by low-temperature ion bombardment by using, for example, oxygen ions 6 as shown in FIG. 4B. This low-temperature ion bombardment is one type of down-flow plasma treatment. This treatment will now be discussed in detail. The semiconductor substrate 1 having the resist film 2 is placed on, for example, an electrode 25 connected to a power supply 31. An ion generator (not shown) is provided above the semiconductor substrate 1.

In carrying out low-temperature ion bombardment on the resist film 2, first, the oxygen ions 6 are generated by the ion generator with the semiconductor substrate 1 of silicon or the like kept at a temperature equal to or lower than, for example, 120 °C. Next, a voltage is applied to the electrode 25 to generate a predetermined electric field which acts toward the semiconductor substrate 1 from the ion generator, thereby applying a predetermined bias to the

ions 6. As a result, the ions 6 are accelerated to collide with the surface of the resist film 2. By this, the hardened layer 4 of the resist film 2 is removed.

Then, as shown in FIG. 4C, the unhardened layer (the remaining resist film) 3 is removed by a high-temperature down-flow plasma treatment while keeping the semiconductor substrate 1 at a temperature equal to or higher than, for example, 120 °C. Specifically, lamp heat 27 is applied to the semiconductor substrate 1 by a heater (not shown) like a heating lamp, provided near the semiconductor substrate 1, and oxygen radicals 18 bombard on the unhardened layer 3. As a result, the unhardened layer 3 is removed.

According to this embodiment, ashing is performed on the hardened layer 4 by low-temperature ion bombardment using oxygen ions without using fluorine ions having a high activity. The oxygen ions efficiently break up the chemical bonding of the dopant and the elements constituting the resist film 2 in the hardened layer 4, producing a volatile hydride. It is therefore possible to efficiently remove the hardened layer 4 without damaging the surface of the semiconductor substrate 1 (the insulation oxide film or the like). As the step of removing the hardened layer 4 is carried out at a low temperature, popping does not occur. This can improve the yield of semiconductor devices.

As apparent from the above, the hardened layer 4 can be removed at a high rate even at a low temperature by applying a bias to the ions. The bias is applied in the level in which the ions does not damage the substrate 1.

Note however that in the step of removing the unhardened layer 3, if the bias is applied to the ions, the semiconductor substrate 1 is damaged by the ions. Therefore, ashing of the unhardened layer 3 is carried out by using a high-temperature down-flow plasma in which no bias is applied to the ions. Consequently, with the hardened layer 4 having already been removed, no popping occurs and the unhardened layer 3 can be removed at a high rate. If a high-density plasma is used as a plasma source, the unhardened layer 3 can be removed at a higher rate.

Although the temperature in the low-temperature ion bombardment is set equal to or lower than 120 °C in this embodiment, setting the temperature equal to or lower than 100 °C can further enhance the effect of preventing the occurrence of popping. Although oxygen ions are generated in the low-temperature ion bombardment in this embodiment, this invention is not limited to such ions. Any gas which does not contain a fluorine, has a relatively large mass and can be ionized may be used as the gas to be supplied to the ion generator. For example, an oxygen gas, a mixed gas of an oxygen gas and nitrogen gas, an argon gas, a helium gas or the like can be used.

Further, the conditions for applying a bias to the ions are not particularly limited, but the proper conditions can be set depending on the type of the gas in use, the thickness of the hardened layer 4 of the resist film 2, the conditions for ion generation by the ion generator, etc. Furthermore, although the unhardened layer

3 is removed by the high-temperature down-flow plasma treatment in this embodiment, the ordinary down-flow plasma treatment may be used as well. In the case of using the high-temperature down-flow plasma treatment, it is preferable to set the temperature equal to or higher than 120 °C.

A method of holding the substrate 1 at a high temperature in the high-temperature down-flow plasma treatment is not particularly limited. For instance, a heater like a heating lamp or a heating panel may be provided in the vicinity of the semiconductor substrate 1. As an alternative way of holding the substrate 1 at a high temperature, a heater for heating a support member (not shown) which support the semiconductor substrate 1 may be provided. Further, the temperature of the semiconductor substrate 1 can easily be controlled by altering the set temperature for the heat generated by the heater or controlling a switch for the heating lamp or the like.

FIGS. 5A through 5C are cross-sectional views illustrating a step-by-step method of removing a resist film having a hardened layer according to the second embodiment of the invention. The second embodiment shown in FIGS. 5A-5C differs from the first embodiment shown in FIGS. 4A-4C only in how to control the temperature of the substrate. To avoid the redundant and detailed description, therefore, like or same reference numerals are given to those components of the second embodiment in FIGS. 5A-5C which are the same as the corresponding components of the

first embodiment shown in FIGS. 4A-4C. As shown in FIG. 5A, as a high dose of arsenic ions 11 is injected in the resist film 2, a hardened layer 4 is formed at the surface of the resist film 2.

Next, with the semiconductor substrate 1 placed in a resist film removing apparatus (not shown), the hardened layer 4 of the resist film 2 is removed by low-temperature ion bombardment as shown in FIG. 5B. At this time, pins 32 are located between the semiconductor substrate 1 and the electrode 25. The pins 32, which are designed to be elevatable up and down as needed, are lifted up in the step of removing the hardened layer 4.

Then, as shown in FIG. 5C, with the pins 32 moved down to make the substrate 1 contact the electrode 25, the unhardened layer 3 is removed by a high-temperature down-flow plasma treatment.

According to the second embodiment, as the pins 32 are lifted up to set the electrode 25, heated by a heater (not shown), apart from the substrate 1 in the step of removing the hardened layer 4, the substrate 1 can be kept at a low temperature. In the step of removing the unhardened layer 3, the pins 32 are elevated downward, making the electrode 25 contact the substrate 1, so that the temperature of the substrate 1 can be raised. By adjusting the temperature of the substrate 1 by upward or downward elevation of the pins 32 or by controlling the ON/OFF action of the switch for the heating lamp or the like, the temperature of the substrate 1 can be increased

more drastically than by altering the set temperature of the heater or the like provided near the substrate 1.

The removing method of the resist film which embodies this invention will now be discussed referring to the flowchart illustrated in FIG. 6. As shown in FIG. 6, first, low-temperature ion bombardment is performed on the hardened layer 4 of the resist film 2 (step 41). Next, it is determined if there is any hardened layer 4 remaining (step 42). If some hardened layer 4 is present (YES), the flow returns to step 41 to continue the low-temperature ion bombardment. If no hardened layer 4 has remained (NO), the flow proceeds to the next step 43. Then, a high-temperature down-flow plasma treatment is performed on the unhardened layer (step 43). It is then determined if any resist film 2 (unhardened layer 3) has remained (step 44). If some resist film 2 exists (YES), the flow returns to step 43 to continue the high-temperature down-flow plasma treatment. If no unhardened layer 3 has remained (NO), the process is terminated.

According to this invention, how to determine if the hardened layer 4 and the unhardened layer 3 have been removed completely is not particularly limited. For instance, a method of always measuring the thicknesses of the hardened layer 4 and the unhardened layer 3 may be used. Alternatively, the thicknesses of the hardened layer 4 and the unhardened layer 3 formed on the surface of the semiconductor substrate 1 to be processed may be measured in advance, the times for the removal of the hardened layer

4 and the unhardened layer 3 may be acquired based on the predetermined speeds of removing the hardened layer 4 and the unhardened layer 3, and the processing times may be monitored based on the acquired removal times. The determination may be accomplished also by analyzing a change in the color of the plasma by unaided eyes or through a spectrum analyzer in the plasma treatment. By using any of those methods, it is possible to stop a predetermined operation and proceed to the next step.

In the case of removing the resist film 2 by the methods of the first and second embodiments, it is preferable to use the principle of the down-flow plasma treatment in space in a predetermined closed state in the low-temperature ion bombardment. For example, if a well-known inductive coupled plasma ashing system is used in the low-temperature ion bombardment, this system can also be used in the later step of removing the unhardened layer 3. This way the hardened layer 4 and the unhardened layer 3 can be removed successively.

FIG. 7 is an exemplary diagram of an apparatus for removing a resist film according to the first embodiment of the invention. FIG. 7 shows a step of removing the hardened layer 4 of the resist film 2. The substrate 1, the electrode 25, etc. shown in FIGS. 5A-5C are placed in a closed chamber 21 incorporating a tank (not shown) which is to be filled with a gas. According to this embodiment, the semiconductor substrate 1 is placed on a support member 28, and the semiconductor substrate 1 is moved up and down by

the pins 32.

A coil (ion generator) 22 is located outside the closed chamber 21 above the substrate 1, with a high-frequency current source 23 connected to the coil 22. As a high-frequency current is supplied to the coil 22, therefore, the gas expelled from the tank can be ionized. A power supply 31 for applying a bias to generated ions 24 is connected to the electrode 25; the electrode 25 and the power supply 31 constitute a bias applying device 26. A temperature controller 30 for controlling the temperature of the substrate 1 is connected to the electrode 25. This temperature controller 30 has a heating lamp 33.

A description will now be given of how to remove the resist film 2 by using the thus structured resist film removing apparatus 20. First, after the substrate 1 is placed on the support member 28 in the closed chamber 21, inside the chamber 21 is held to a predetermined vacuum state. Further, the tank is filled with an oxygen gas as a gas for generating the ions 24. Beside the oxygen gas, a mixed gas of an oxygen gas and nitrogen gas, or an argon gas or a helium gas can be used as well. Next, the gas is expelled from the tank and a high-frequency current is supplied to the coil 22, thus generating the ions 24. At this time, a voltage is applied to the electrode 25 to apply a bias of, for example 100 to 300 W to the ions 24 in such a direction as to accelerate the ions 24 toward the hardened layer 4. The pins 32 are at the lifted-up position, separating the substrate 1 from the electrode 25, so that

the temperature of the substrate 1 is held at a temperature ranging from, for example, the room temperature to 100 °C. As the low-temperature ion bombardment is performed on the substrate 1 in this manner, the hardened layer 4 is removed.

Next, the application of the voltage to the electrode 25 is stopped, and the process is switched to the down-flow plasma treatment. To keep the temperature of the substrate 1 at a temperature higher than that in low-temperature ion bombardment, for example, in the temperature range from 150 °C to 300 °C, at this time, the pins 32 are moved downward to cause the substrate 1 to come closer to the heating lamp 33. As the down-flow plasma treatment is carried out on the substrate 1 in this manner, the unhardened layer 3 is removed.

Although the temperature of the substrate 1 is controlled by the heating lamp 33 and the upward and downward elevation of the pins 32 in this embodiment, the way of controlling the temperature of the substrate 1 is not limited to this particular type in this invention.

FIG. 8 is an exemplary diagram showing an apparatus for removing a resist film according to the second embodiment of the invention. To avoid the redundant and detailed description, like or same reference numerals are given to those components shown in FIG. 8 which are the same as the corresponding components in FIG. 7. FIG. 8 shows a step of removing the unhardened layer 3 of the resist film 2. According to the second embodiment, as shown in FIG. 8, the electrode 25 also serves as a heat source

for heating the semiconductor substrate 1. The temperature of the substrate 1 can therefore be adjusted by controlling the temperature of the electrode 25 by the temperature controller 30.

Although the coil 22 is used as the ion generator in the first and second embodiments, the type of that device is not limited in this invention as long as it is capable of ionizing the gas filled in the tank. Although the electrode 25 is provided as means for applying a bias to the ions 24, the type of that means is not limited if it can apply an electric field in such a direction to accelerate the ions 24 toward the substrate 1.

According to the first and second embodiments, the low-temperature ion bombardment and down-flow plasma treatment can be carried out in the same chamber using the same gas, and the hardened layer 4 and the unhardened layer 3 can be removed successively. This can permit the removal of the resist film at a high throughput without resulting in an increased cost.

The results of the removal of the resist film by the method according to the first embodiment of the invention will be discussed below specifically. The resist film 2 is formed about 1 μm thick on the surface of the semiconductor substrate 1 in advance, and arsenic ions are injected in the resist film 2 at a dose of $5 \times 10^{15}/cm^2$ and 60 eV, forming the resist film 2 consisting of the hardened layer 4 and unhardened layer 3, as shown in FIG. 4A.

Next, ashing of the hardened layer 4 is carried out

by using an inductive coupled plasma ashing system as shown in FIG. 4B. The ashing conditions were the RF power of 900 W, a bias of 200 W, the pressure of 1.1 Torr in the chamber, the flow rate of the oxygen gas (O_2) of 3750 sccm and the stage (electrode) temperature of 100 °C. It is to be noted that the temperature of the substrate 1 is 100 °C and the scraping speed for the hardened layer 4 is approximately 4 μm/min. If the low-temperature ion bombardment is performed on the hardened layer 4 under those conditions, because of a bias applied to the high-density plasma, the hardened layer 4 can be removed by using only the oxygen gas.

Then, as shown in FIG. 4C, with the substrate 1 placed in the same chamber as used in the low-temperature ion bombardment, the process is switched to the down-flow plasma treatment with a bias of 0 W and lamp heat 27 is applied to the substrate 1 by the heating lamp. The temperature of the substrate 1 then becomes 150 °C and the scraping speed for the unhardened layer 3 is approximately 3 μm/min. This can allow the unhardened layer 3 to be removed without damaging the substrate surface.

Now, the results of the removal of the resist film by the method according to the second embodiment of the invention will be discussed specifically. The resist film 2 is formed about 1 μm thick on the surface of the semiconductor substrate 1 in advance, and arsenic ions are injected in the resist film 2 at a dose of $5 \times 10^{15}/cm^2$ and 60 eV, forming the resist film 2 consisting of the hardened layer 4 and unhardened layer 3, as shown in FIG. 5A.

Next, ashing of the hardened layer 4 is carried out by using an inductive coupled plasma ashing system as shown in FIG. 5B. The ashing conditions were the RF power of 900 W, a bias of 200 W, the pressure of 1.1 Torr in the chamber, the flow rate of the oxygen gas (O_2) of 3750 sccm and the stage (electrode) temperature of 200 °C. It is to be noted that as the substrate 1 is held apart from the stage by the pins 32, the temperature of the substrate 1 becomes 80 °C. The scraping speed for the hardened layer 4 is approximately 4 μm/min. By performing the low-temperature ion bombardment on the hardened layer 4 under those conditions, the hardened layer 4 can be removed, exposing the unhardened layer 3.

Then, as shown in FIG. 5C, with the substrate 1 placed in the same chamber as used in the low-temperature ion bombardment, the process is switched to the down-flow plasma treatment with a bias of 0 W and the pins 32 are moved downward to make the substrate 1 contact the stage (electrode) incorporating a heater. The temperature of the substrate 1 then becomes 200 °C and the scraping speed for the unhardened layer 3 is approximately 4 μm/min. This can allow the unhardened layer 3 to be removed without damaging the substrate surface.

As apparent from the above, the use of the method according to the second embodiment can permit the substrate 1 to receive heat directly from the high-temperature stage, so that the unhardened layer 3 can be removed at a higher rate than the one accomplished by the method of the first

embodiment which applies the lamp heat 27.

Each feature disclosed in this specification (which term includes the claims) and/or shown in the drawings may be incorporated in the invention independently of other disclosed and/or illustrated features.

The text of the abstract filed herewith is repeated here as part of the specification.

A resist film is formed on a semiconductor substrate, with a hardened layer formed at the surface of this resist film by ion implantation. First, oxygen ions are generated by an ion generator while the semiconductor substrate placed on an electrode is kept at a temperature equal to or lower than, for example, 120°C. Next, a voltage is applied to the electrode to generate a predetermined electric field which acts toward the semiconductor substrate from the ion generator, thus applying a predetermined bias to the ions. As low-temperature ion bombardment is performed on the resist film by using the oxygen ions, the hardened layer is removed. Then, the remaining resist film is removed by a down-flow plasma treatment.

CLAIMS

1. A method of removing a hardened layer of a resist film on a surface of a semiconductor substrate, comprising providing positively charged ions, maintaining the surface negatively biassed relative to said ions, and at a temperature low enough to avoid popping (as hereinbefore defined), and bombarding the hardened layer with said ions to remove it.

2. A method of removing a hardened layer at a surface of a resist film formed on a semiconductor substrate by low-temperature ion bombardment in which a surface of said semiconductor substrate is negatively charged, kept at 120°C or below and positively charged ions are showered onto said hardened layer.

3. The method according to claim 1 or claim 2, wherein said hardened layer is formed by ion implantation in said resist film.

4. The method according to claim 1 or claim 2, wherein said ion bombardment includes the steps of:

keeping the temperature of said semiconductor substrate at 120°C or below;

generating ions to be bombarded on said resist film; and

applying a bias to said ions, whereby said ions are showered on said surface of said resist film to remove said hardened layer.

5. The method according to claim 4, wherein said bias applying step includes a step of applying a bias of 100 to 300 V to said ions.

6. The method according to claim 1 or claim 2, wherein said ions are produced from oxygen, or a mixture of oxygen and nitrogen, or argon or helium.

7. The method according claim 1 or claim 2, further comprising, after said step of removing said hardened layer, a step of removing said resist film, remaining after removal of said hardened layer, by a down-flow plasma treatment in which no bias is applied to said ions.

8. The method according to claim 6, wherein said down-flow plasma treatment is carried out while keeping said semiconductor substrate at a temperature higher than that of said semiconductor substrate in said low-temperature ion bombardment.

9. The method according to claim 8, wherein said down-flow plasma treatment is performed while keeping said semiconductor substrate at a temperature equal to or higher than 120°C.

10. The method according to claim 9, wherein said down-flow plasma treatment is performed while keeping said semiconductor substrate at a temperature between 150°C and 300°C.

11. The method according to claim 7, wherein said low-temperature ion bombardment and said down-flow plasma treatment are carried out by using same ions.

12. An apparatus for removing a resist film having a hardened layer, comprising:

a closed chamber where a semiconductor substrate is to be placed;

an ion generator for generating ions in said closed chamber;

a bias applying device for applying a bias to positively charged ions with a surface of said semiconductor substrate being negatively biased; and

a temperature controller for controlling a temperature of said semiconductor substrate.

13. The apparatus according to claim 12, wherein low-temperature ion bombardment for showering said ions onto said surface of said semiconductor substrate kept at 120°C or below and a down-flow plasma treatment in which no bias is applied to said ions are performed in said closed chamber, and in said down-flow plasma treatment, said temperature controller keeps said semiconductor substrate at a temperature higher than that of said semiconductor substrate in said low-temperature ion bombardment.

14. The apparatus according to claim 13, wherein said temperature controller keeps said semiconductor substrate at a temperature equal to or lower than 120°C in said low-temperature ion bombardment.

15. The apparatus according to claim 13, wherein said temperature controller keeps said semiconductor substrate at a temperature equal to or higher than 120°C in said down-flow plasma treatment.

16. The apparatus according to claim 12, wherein said bias applying device forms such an electric field as to accelerate said ions toward said resist film on said semiconductor substrate.

17. The apparatus according to claim 12, wherein said temperature controller has a heat source for heating said semiconductor substrate.

18. The apparatus according to claim 17, wherein said temperature controller has a distance adjuster for adjusting a distance between said semiconductor substrate and said heat source.

19. The apparatus according to claim 11 or claim 12, wherein said closed chamber has a tank for supplying one kind of gas selected from an oxygen gas, a mixed gas of an oxygen gas and nitrogen gas, an argon gas and a helium gas into said closed chamber.

20. A method of or apparatus for removing a hardened layer of a resist film substantially as herein described and/or as shown in any of figures 4 to 8 of the accompanying drawings.

The Patent Office

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): G2X(XB5D),H1K(KLX)

Int Cl (Ed.6): G03F 7/42,H01L 21/311

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0386609A	(Fujitsu)(Figs)	1 and 3 at least
X	EP 0367568A	("")(Figs, Col 7 lines11-23)	""
X	EP 0320045A	("")(Figs, esp Fig 5 and page 6 line 53-page 7 line 2)	""
X	EP 0304068A	("")(Figs)	1-4,7 at least
X	US 5268056	(Matsushita)(Figs, esp Fig 7 and Col 6)	1 and 12 at least
X	US 5226056	(Nihon)(Figs, esp Figs 16-17 and Cols 9-10)	""

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